

Wireless LAN and Bluetooth[®] Module

WYSBHVXG

Application Note

In case you adopt this module and design some appliance, please ask for the latest specifications to the local sales office.

Table of content

- Revision log
- 1. Overview
- 2. Scope
- 3. Summary description of this module
 - 3-1. Module configuration
- 4. Design guide
 - 4-1. Power start up sequence
 - 4-2. Clock sequence
 - 4-3. Recommended power circuit
 - 4-4. Pattern design guide
 - 4-4-1. Power supply system
 - 4-4-2. Bypass capacitor layout
 - 4-4-3. Clock input
 - 4-4-4. Recommended pattern on RF part
 - 4-4-5. GND pattern
 - 4-4-6. Antenna matching
 - 4-4-7. Digital I/F related issue
 - 4-4-8. Unused terminal processing
 - 4-4-9. Mounting land pattern dimension
 - 4-5. Heat consideration
- 5. Storing calibration data
- 6. Caution on mounting
- 7. Certification
 - 7-1. Radio Law Qualification
- 8. Explanation on software
 - 8-1. Software configuration and type
 - 8-2. Type of NXP standard driver
 - 8-3. License agreement
 - 8-4. Caution on WLAN driver install
 - 8-4-1. Driver porting
 - 8-4-2. SDIO controller

Revision log

Revision	Date	Change history
Version 1.0	11-Mar. 2016	Original release
Version 1.1	27-Mar. 2017	Minor change
Version 1.2	24-Jun. 2020	Modified section 8.

WYSBHVXG

TAIYO YUDEN CO., LTD.

1. Overview

The content of this material is design guideline to provide stable characteristics of wireless communication module which is developed and sold by TAIYO YUDEN CO., LTD. It is technical data for the purpose of utilization in designing of equipment which adopt module, and module peripheral circuit.

In case of designing peripheral circuit or equipment with reference to this material, please make full evaluation of module characteristics at customer's premises before practical application. For any inquiry, please contact our staff.

2. Scope

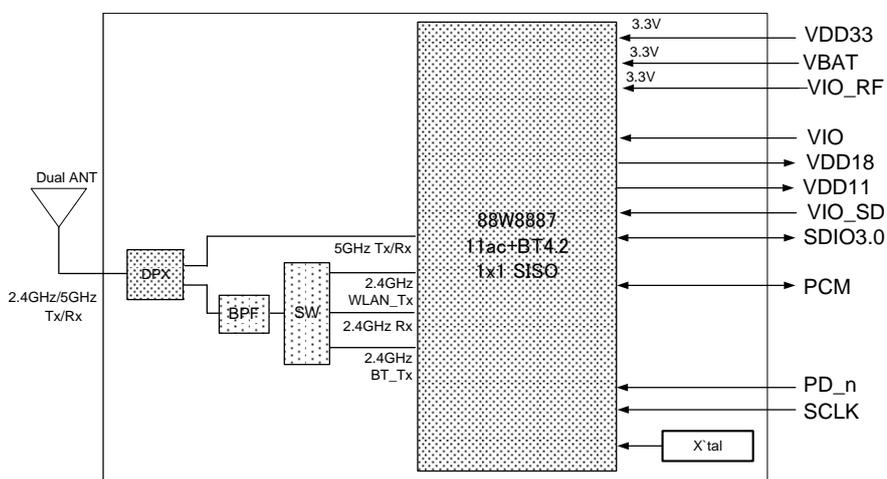
The content of this material is applicable to following product of wireless communication module.

Objective item: WYSBHVXG

3. Summary description of this module

This is module with hybrid functionality adopting 88W8887 by NXP. It is compact module with multifunction, compliant to IEEE802.11ac/a/b/g/n and *Bluetooth4.2*[®], and possesses interface such as SDIO. For detailed information, please obtain and check the latest Data Report.

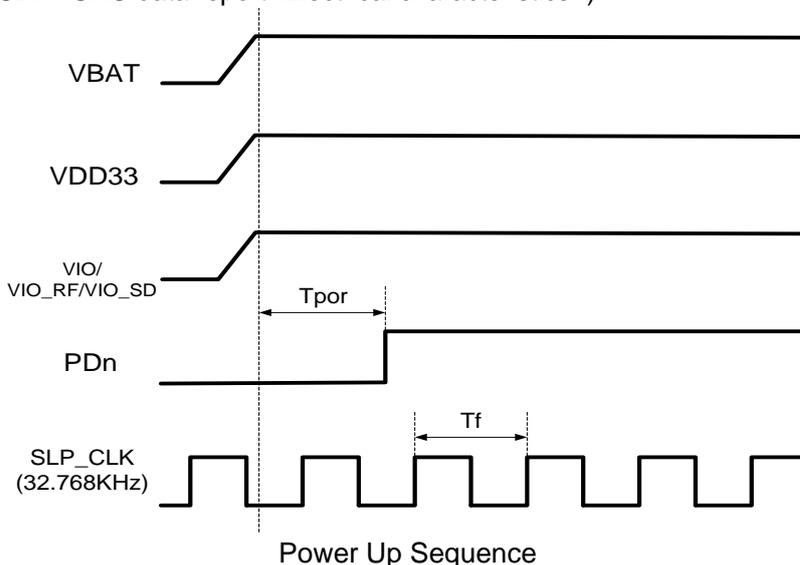
3-1. Module configuration



4. Design guide

4-1. Power start up sequence

PDn must maintain a low level for Tpor (at least 300msec.) after power supply voltage is recommend voltage to actuate POWER ON RESET and make normal start up of module. (Reference: WYSBHVXG data report "Electrical characteristics".)



WYSBHVXGXG

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4-2. Clock sequence

SLP_CLK is used for detecting fast clock setting and for operation of sleep mode.

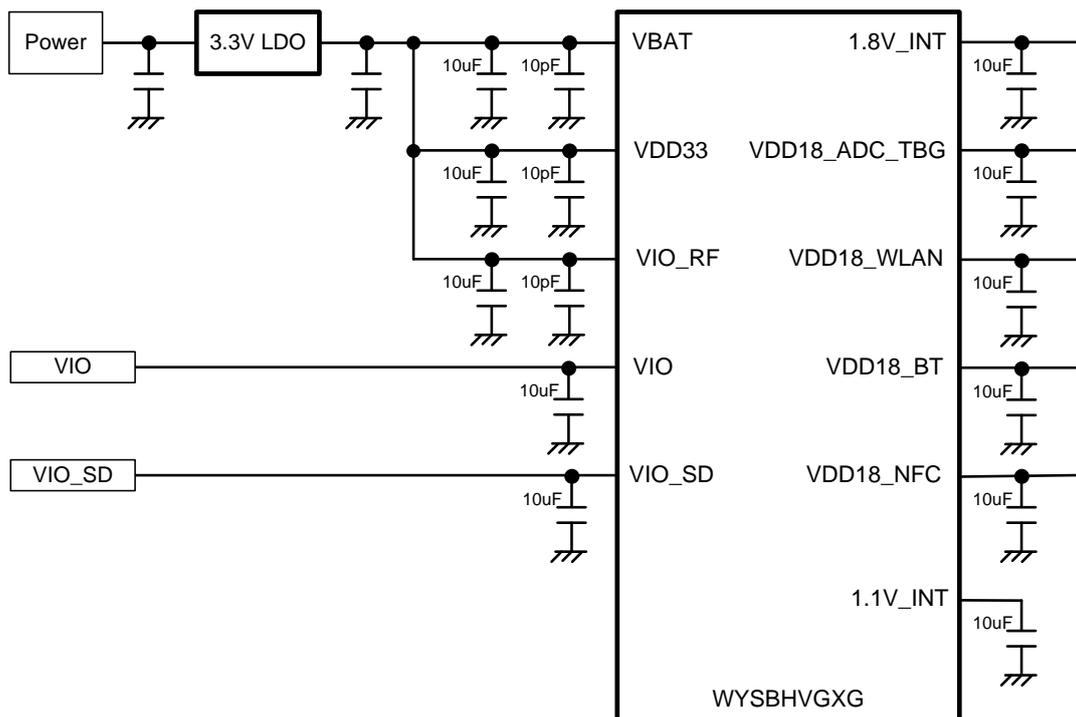
Clock signal shall be input Tf (32.768kHz) to SLP_CLK(1.8V).

(Reference: WYSBHVXGXG data report “Electrical characteristics”.)

4-3. Recommended power circuit.

There are power supplies for buck convertor (VBAT), analog circuit (VDD33, VDD18_ADC_TBG, VDD18_WLAN, VDD18_BT and VDD18_NFC), and Digital I/F (VIO, VIO_SD).

<Typical configuration with LDO>



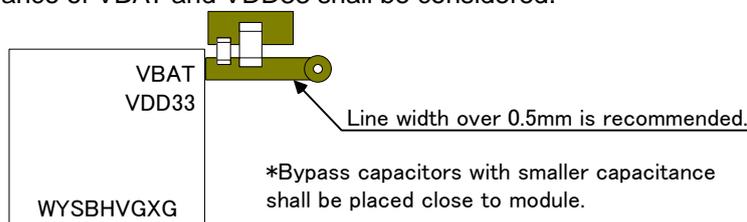
- For VBAT, VDD33 and VIO_RF rated output current over 760mA.
(Example in 3.3V LDO: S-1172B33-E6T1G (ABLIC Inc.))
- The bypass capacitors for LDO shall be placed close to the input/output terminals.
- The bypass capacitors for all supply terminals shall be placed close to the terminals.
- Input ripple to VBAT, VDD33 and VIO_RF shall be under 50mVp-p.
- * During board designing, please pay attention to power dissipation.
- We recommend that you use the internal buck convertor (1.8V_INT) for analog circuit (VDD33, VDD18_ADC_TBG, VDD18_WLAN, VDD18_BT and VDD18_NFC).

4-4. Pattern design guide

4-4-1. Power supply system

Bypass capacitors on each power supply line shall be placed close to power supply terminals of this product. Since capacitance will be affected by quality of power supply, optimum constant shall be required.

Line width allowance of VBAT and VDD33 shall be considered.



4-4-2. Bypass capacitor layout

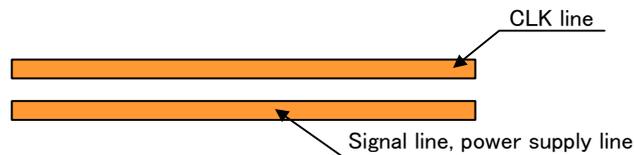
Bypass capacitor shall be grounded in combination of small capacitance (about 10pF), large capacitance (1uF to 10uF). GND of bypass capacitor shall be close to adjacent module GND to enable shortest closed loop.

4-4-3. Clock input

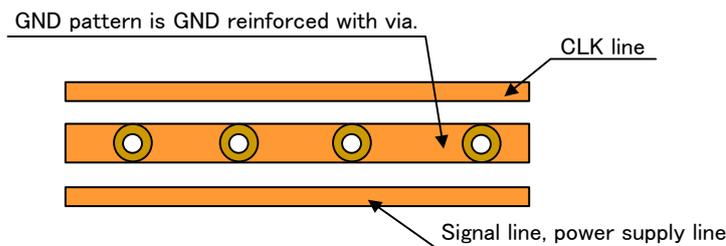
In order to stabilize RF characteristics and reduce spurious, clock signal line shall be designed to be shortest with isolation from adjacent pattern by GND.

CLK line, signal line and power supply line shall be placed away each other. Parallel placement shall be avoided. In case of parallel placement due to design restriction, in-between GND pattern shall be placed for isolation. In case of proximity between layers, GND layer shall be placed.

<Bad example>

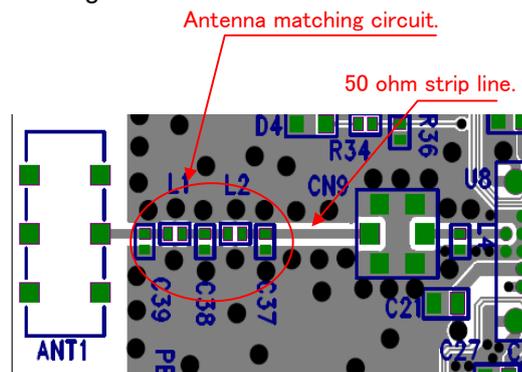


<Good example>



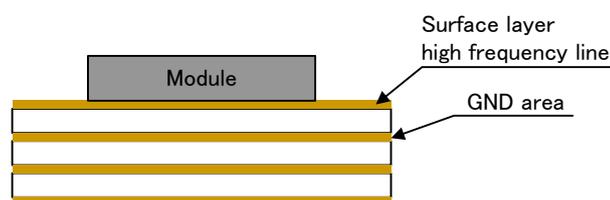
4-4-4. Recommended pattern on RF part

RF output impedance for this product is 50 ohm. In case of patterning to antenna, please make design of RF line as 50 ohm strip line. Please keep the area and land pads for matching elements to be placed for ensuring matching with antenna.



4-4-5. GND pattern

Bypass capacitor GND for power supply line, etc. shall be placed in proximity of this product GND. Wide GND area shall be reserved to ensure isolation for each layer.

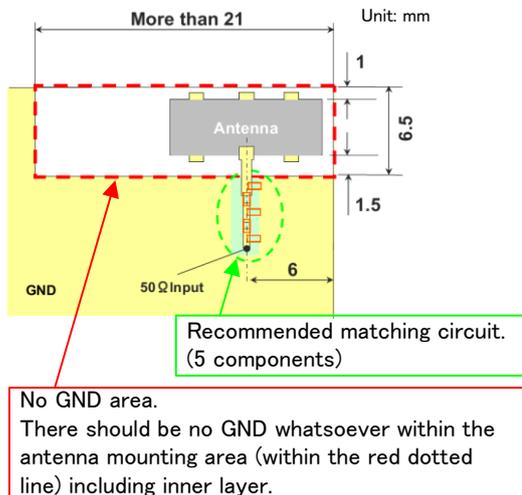


GND pattern of each layer shall be connected to GND area with large number of via.

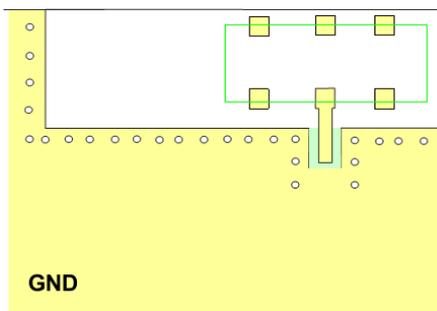
4-4-6. Antenna matching

Recommended antenna is **AH104N2450D1** (2G/ 5GHz band compliant antenna) made by TAIYO YUDEN CO., LTD.. Antenna location, peripheral configuration and matching circuit have significant effect on radiation characteristics. Please observe following antenna peripheral design guide. Support is available in antenna peripheral design.

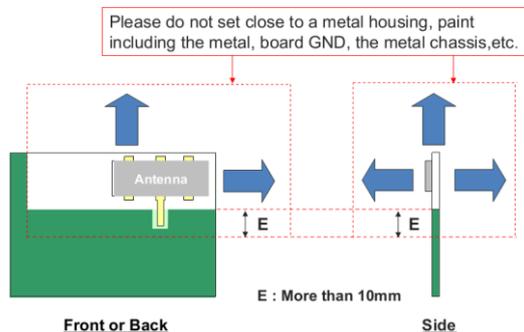
<Recommended pattern layout>



<Example of through hole>



<Metal avoidance area>



4-4-7. Digital I/F related issue

<In the case of SDIO>

On pattern design of SDIO line between module and HOST, pay attention to following items.

- Each SDIO line between this product and HOST should be routed with the same length as short as possible and must be parallel and symmetrical. GND via shall be set between each line (especially SD_CLK) for shielding.
- In case of long wiring or connector/FPC application between boards, effect of reflection shall be eliminated by making series insertion of dumping resistor, etc. to each line as necessary.
- It shall be away from pattern such as each RF line and shall not overlap with these signals.
- For other digital signals, they shall be away from SD_CLK, and shall not overlap with these signals between layers.

4-4-8. Unused terminal processing

Unused terminals (RES terminal, unconnected terminal) shall be open in circuit, and land under module shall be created.

4-4-9. Mounting land pattern dimension

Please refer to recommended land pattern specified in Data Report.

4-5. Heat consideration

Under high temperature, this product could not offer sufficient performance. Therefore, this product placement shall be designed to avoid effect from circuit or device which may be thermal source in customer's product. Also, connection to GND layer on PCB of customer's product (via through-hole, etc.) shall be made to ensure effective heat dissipation of module.

5. Storing calibration data

The calibration data needs to be stored in a configuration file or OTP. Although originally driver requires the configuration file, in the case of this product, it is not necessary to set the configuration file, as the calibration data is stored in OTP.

When driver is installed to this product, please execute the following command.

Please set "none" for cal_data_cfg.

```
"insmod sd8887.ko cal_data_cfg=none"
```

6. Caution on mounting

For mounting of this product, please refer to recommended reflow profile specified in data report.

7. Certification**7-1. Radio Law Qualification**

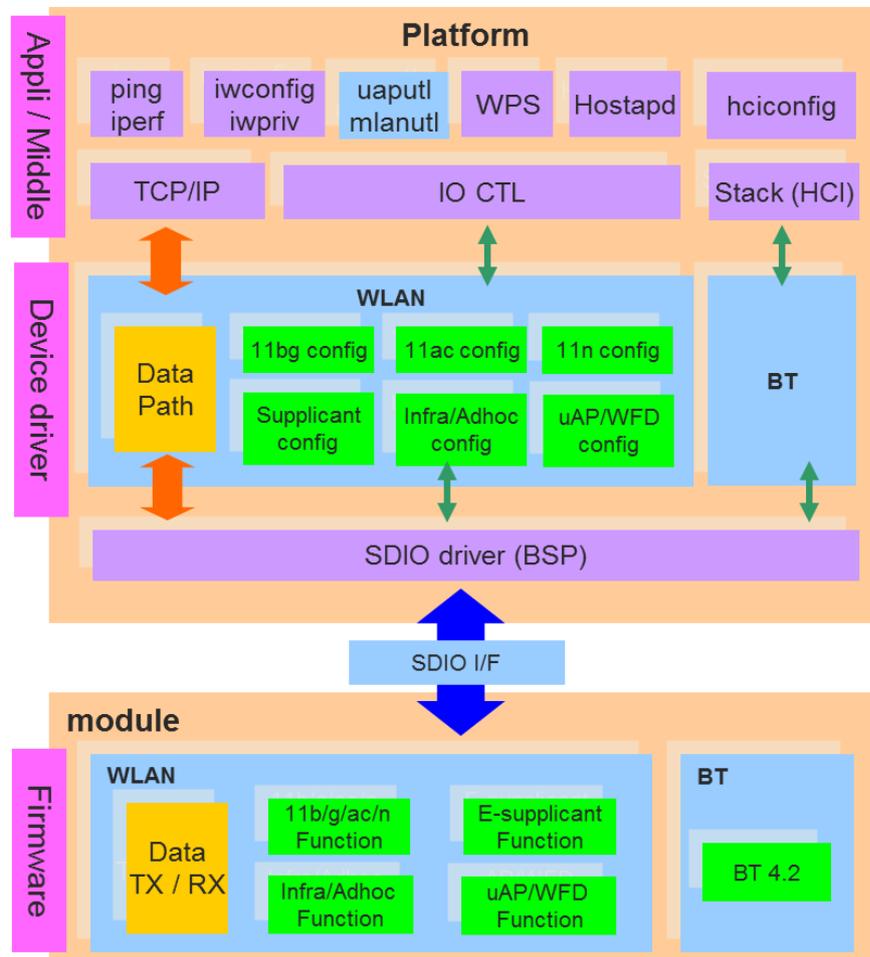
In order for the customer to market the product, it is required to obtain Radio Law Qualification for each country on customer's product. To obtain Radio Law Qualification, it is required to perform certification test on equipment, and there are points to be considered in hardware and software.

For RF characteristics measurement, it is required to mount RF connector between module and matching circuit. Please refer to circuit diagram of evaluation board, and component table.

In order to test module, it is required to install software for control into the product. For details, please make inquiry to the provider of driver software.

8. Explanation on software

8-1. Software configuration and type



➤ *Firmware and driver:*

The firmware and driver package are provided by TAIYO YUDEN CO., LTD. under the license agreement. It includes *uaputl* application for access-point function and *mlanutl* application for Infrastructure function.

➤ *Supplicant :*

Embedded supplicant is implemented in Firmware. Alternatively, open source *wpa_supplicant* / *hostapd* are available as external supplicant. The choice is up to your application.

8-2. Type of NXP standard driver

As below table, Linux driver for x86 architecture. Linux 2.6.32 up to 5.2.9.

For other CPU/OS, you can port because the source code is provided. We can also introduce partner companies that do various porting, etc.

[NXP standard driver]

CPU / OS	I/F	Providing method
x86 + Ubuntu16.04	SDIO	Source code

8-3. License agreement

To obtain source code package, you shall close a contract of SLA (Software License Agreement) with NXP or TAIYO YUDEN CO., LTD..

* As for object package, SLA is not required.

8-4. Note on driver install**8-4-1. Precondition**

To run WLAN driver, following function is required.

- SDIO

8-4-2. SDIO controller

One of the important factors for WLAN throughput is SDIO3.0-Clock frequency. In our experience, better throughput at 150MHz or higher.

It is recommended that SD controller specification of the product satisfy the following.

- SDIO3.0: SDIO-Clock, more than 150MHz, SDIO-Bus 4bit mode
- Data transfer system: Multi-Block transfer support by DMA